IN THE CLAIMS

Please amend the claims as follows.

1. (Cancelled).

2. (Previously Presented) A system for allowing shared access by at least two processors including an embedded controller and a host processor to at least two modules, comprising:

a transaction control, wherein the embedded controller is capable of providing an indication of which of the modules to access to the transaction control, and wherein the host processor is capable of providing an indication of which of the modules to access to the transaction control; and

at least one access block bit controlled by one of the processors for blocking access by another of the processors to at least one of the modules, wherein the at least one access block bit is capable of enabling at least one of the modules.

3. (Cancelled).

4. (Previously Presented) The system of claim 2, further comprising a bus extension;

wherein at least one of the modules is accessible via said bus extension;

wherein said transaction control is capable of providing to said bus extension an indication of said at least one of the modules, accessible via said bus extension, for access by the host processor;

wherein said transaction control is capable of providing to said bus extension an indication of said at least one of the modules, accessible via said bus extension, for access by the embedded controller; and

wherein said bus extension is capable of providing an indication of said at least one of the modules for access by one of the processors.

5. (Previously Presented) The system of claim 2, wherein said transaction control is capable of providing an indication of at least one of the modules for access by one of the processors.

6. (Previously Presented) The system of claim 2, wherein at least one of the modules is part of an input/output chip.

Claims 7-49 (Cancelled).

50. (Previously Presented) A method for allowing shared access to at least two modules by at least two processors including an embedded controller and a host processor, comprising the steps of:

receiving an indication from each of the processors of a module from among the at least two modules to access;

arbitrating between the processors in favor of one of the processors, wherein arbitrating between the processors comprises allowing one of the processors to control at least one access block bit, the at least one access block bit capable of blocking access by another of the processors to at least one of the modules, the at least one access block bit capable of enabling at least one of modules; and

accessing said module indicated by said one of the processors.

51. (Previously Presented) The method of claim 50, further comprising the step of:

blocking access by another of the processors to said module indicated by said one of the processors.

52. (Previously Presented) The method of claim 50, wherein said indication from each of the processors is for a different module to access.

53. (Previously Presented) A method for allowing a processor comprising an embedded controller to access at least two modules affiliated with a device, comprising the steps of:

indicating the device;

indicating an access direction (read/write);

indicating one of the modules for accessing;

indicating a location for accessing, within said indicated one of the modules;

transferring data between said indicated location and the embedded controller; and

setting at least one access block bit to block access by another processor to at least one of the modules, wherein the at least one access block bit is capable of enabling at least one of the modules.

54. (Previously Presented) The method of claim 53, wherein said indicated one of the modules is accessible via a bus extension.

55. (Previously Presented) The method of claim 54, wherein said step of indicating one of the modules for accessing includes the step of:

indicating one of at least one chip select corresponding to said bus extension for accessing.

56. (Previously Presented) The method of claim 53, wherein said indicated one of the modules is part of an input/output chip.

57. (Previously Presented) The method of claim 56, wherein said step of indicating one of the modules for accessing includes the step of:

indicating a logical device number.

58. (Previously Presented) The method of claim 53, wherein said step of indicating a location for accessing includes the step of providing an indication of a location for accessing via an internal bus to said indicated one of said modules, the method further comprising the step of:

waiting for a freeing up of said internal bus before transferring said indication of a location for accessing onto said internal bus.

59. (Previously Presented) The method of claim 58, wherein said internal bus is occupied by a transaction originating from the other processor prior to said freeing up.

60. (Previously Presented) The method of claim 53, further comprising the step of:

the embedded controller waiting for receipt of data from said indicated location prior to initiating a subsequent access.

Claims 61-69 (Cancelled).

70. (Previously Presented) The system of Claim 4, wherein at least one of the modules comprises a memory accessible through the bus extension.

71. (Previously Presented) The method of Claim 50, wherein at least one of the modules comprises a memory accessible through a bus extension.

72. (Cancelled).

73. (Cancelled).

74. (Currently Amended) The system of Claim 2~~-1~~, wherein the transaction control is further capable of allowing concurrent access by the processors to at least one of: one or more of the modules, and one or more sub-modules within at least one of the modules.

75. (Currently Amended) The system of Claim 2~~1~~, further comprising:

at least one disable bit controlled by one of the processors, wherein the at least one disable bit is capable of disabling at least one of the modules even if the at least one access block bit is set to enable the at least one module; and

at least one tri-state bit controlled by one of the processors, wherein the at least one tri-state bit is capable of disabling an output of at least one of the modules even if the at least one access block bit is set to enable the at least one module.

76. (Currently Amended) The system of Claim 2~~1~~, wherein the at least one access block bit is capable of enabling at least one of the modules by activating the at least one module.